AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-12 (Canceled)

13. (New) An interface receiver coupled among a plurality network elements of at least one network, comprising at least one random access memory (RAM) and at least one comparator, wherein a plurality of data frames comprising information of at least one switching event are received from each of a plurality of channels of a backplane network, wherein compare operations are performed at prespecified intervals among at least one data frame stored in the RAM and at least one subsequently received data frame, wherein at least one interrupt signal is generated in response to data changes determined by the compare operations.

14. (New) The interface receiver of claim 13, wherein the compare operations comprise receiving and storing a first data frame in the at least one RAM, receiving a second data frame into the comparator, reading the first data frame from the RAM, and comparing bits of the first and second data frames.

15. (New) The interface receiver of claim 14, wherein storing comprises multiplexing the plurality of data frames from the plurality of channels into at least one memory area of at least one dual port random access memory (RAM).

16. (New) The interface receiver of claim 14, wherein storing comprises multiplexing the plurality of data frames into at least one field-programmable gate array (FPGA).

17. (New) The interface receiver of claim 13, wherein the plurality of data frames are stored in at least one area of the RAM accessed using at least one memory map, wherein the at least one area of the RAM is distributed among the plurality of network elements.

18. (New) The interface receiver of claim 13, wherein generation of the at least one interrupt signal comprises:

generating at least one unit interrupt signal in response to the data changes;

generating at least one memory map in response to the at least one unit interrupt signal; and

generating at least one massive interrupt signal in response to the at least one unit interrupt signal.

19. (New) The interface receiver of claim 18, wherein the at least one memory map comprises memory maps in a plurality of areas of the RAM.

20. (New) The interface receiver of claim 13, wherein generation of the at least one interrupt signal comprises:

setting at least one unit interrupt bit in a corresponding location of a first RAM in response to at least one detected bit difference resulting from the compare operations;

setting at least one interrupt status bit in a corresponding location of a second RAM area in response to the set at least one unit interrupt bit; and

generating a massive interrupt signal in response to at least one set unit interrupt bit.

21. (New) The interface receiver of claim 13, wherein the data changes include an inequality among bits of the compared at least one data frame.

22. (New) The interface receiver of claim 13, wherein the plurality of data frames comprise approximately 67.5 bytes including status bytes and a plurality of Synchronous Optical Network (SONET) bytes including K1, K2, E1, and F1 bytes transferred as a serial bit stream at a rate of approximately 4.32 megahertz.

23. (New) The interface receiver of claim 13, wherein the backplane network further couples the interface receiver to at least one transmitter, at least one other receiver, and at least one processor, wherein the at least one backplane comprises a 16-channel bus.

24. (New) The interface receiver of claim 23, wherein the at least on processor includes a plurality of processors distributed among the plurality of network elements.

25. (New) The interface receiver of claim 13, wherein protection switching is controlled in the at least one network by at least one processor in response to the at least one interrupt signal, wherein the at least one processor navigates among a plurality of memory locations of the at least one RAM using a plurality of memory maps in response to the at least one interrupt signal,

reads data from the plurality of memory locations relating to switching event information, and evaluates the switching event information.

26. (New) The interface receiver of claim 13, wherein the at least one RAM comprises at least one area including at least one interrupt mask.

27. (New) The interface receiver of claim 13, further comprising at least one serial-to-parallel data converter.